PVP 14

Code: CS4T5

II B.Tech - II Semester–Regular/Supplementary Examinations–April 2018

COMPUTER ORGANIZATION
(COMPUTER SCIENCE & ENGINEERING)

Duration: 3 hours Max. Marks: 70

PART – A

Answer ***all*** the questions. All questions carry equal marks

11 x 2 = 22 M

1. a) Define computer organization and computer architecture.
   b) Explain about combinational circuits.
   c) Explain about two stack operations.
   d) Convert this into reverse polish notation.

      (A + B) * [C * (D + E) + F]

   e) Write short notes on data transfer instructions.
   f) Write short notes on priority interrupt.
   g) With neat diagram how the data transfer done I/O device to CPU.
   h) Explain memory hierarchy in computer system with neat diagram.
   i) Write short notes on multiprogramming.
   j) Explain characteristics of multiprocessors?
   k) Write short notes on LRU.

PART – B

Answer any ***THREE*** questions. All questions carry equal marks.
3 x 16 = 48 M

2. Given the Boolean function 16 M

F =xy'z + x'y'z + xyz

i) List the truth table of the function.

ii) Draw the logic diagram using the original Boolean expression.

iii) Simplify the algebraic expression using Boolean algebra.

iv) List the truth table or the function from the simplified expression and that is the same as the truth table, in part (i) for the given boolean function.

v) Draw the logic diagram from the simplified expression and compare the total number of gates with the diagram of part (ii) for the given boolean function

3. a) Define instruction format. Explain about one address and zero address Instruction Formats. 6 M

b) Write a program to evaluate the arithmetic statement:
10 M

X = (A - B + C * (D * E – F)) / (G + H * K)

i) Using a general register computer with three address instructions.

ii) Using a general register computer with two address instructions.

iii) Using an accumulator type computer with one address instructions.

iv) Using a stack organized computer with zero-address operation instructions.

4. a) Discuss about daisy chaining priority with diagrams. 8 M

b) Explain about DMA controller and DMA transfer with diagrams. 8 M

5. a) Expalin the concept of associative memory. 7 M

b) 9 M

i) How many 128 x 8RAM chips are needed to provide a memory capacity of 2048 bytes?

ii) How many lines of the address bus must be used to access 2048 bytes of memory? How many of these lines will be common to all chips?

iii) How many lines must be decoded for chip select? Specify the size or the decoders.

6. Explain about serial and parallel arbitration procedures in inter processor arbitration. 16 M